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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rajski et al.
Application No. 10/781,031
Filed: February 17, 2004
Confirmation No. 2828
For: METHOD FOR SYNTHESIZING LINEAR FINITE STATE MACHINES
Examiner:
Art Unit: 2124
Attorney Reference No. 1011-67627-01

CERTIFICATE OF MAILING

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450 on the date shown below.

Attorney for Applicants

Date Mailed 12/30/04

INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 C.F.R. § 1.97(b)(3)

COMMISSIONER FOR PATENTS
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ALEXANDRIA, VA 22313-1450

Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language and/or non-English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent.

Copies of United States patents and United States published patent applications do not have to be provided to the Patent Office (37 C.F.R. 1.98(a)(2)(ii)). Copies of unpublished U.S. applications do not have to be provided, as long as the application is available on PAIR, as this requirement of 37 C.F.R. § 1.98(a)(2)(iii) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on October 19, 2004 (1287 OG 163). Applicants will provide copies of such patents or applications upon request.

Further, several foreign language documents are cited in the accompanying form PTO-1449. Specifically, Japanese Patent Publication Nos. 4-236378, 11-153655, and 9-130378 are cited. The abstract of Japanese Patent Publication No. 4-236378 recites that "a method and apparatus for testing a VLSI device 10 are described. The invention uses the idea that the internal logic of the VLSI device can be broken down into linked sections or cones. . . . The apparatus incorporates a Linear Feedback Shift Register (300) which is fed by a seed to produce a bit pattern to test the VLSI device (10). The seed is so chosen that the LFSR generates the required bit values on the input latches 30 which are required for the particular test being carried out and pseudo-random values for all other latches." The abstract of Japanese Patent Publication

No. 11-153655 recites that the problem to be solved by the disclosed invention is "to provide an IC chip inspection device which inspects IC chips by using test data composed of many test vectors." The disclosed invention is "[a]n IC chip inspection device . . . with a pin memory, a sequencer memory, and a driving section. The pin memory stores many test blocks and each test block is the combination of at least one test vector among text [sic] vectors and repeated at least one time in test data. The sequencer memory stores the information on the designating order of the test blocks for restoring the test data." Japanese Patent Publication No. 9-130378 is understood to disclose a process for pledging data for a secure data-exchange protocol that has nothing to do with testing integrated circuits. The disclosed method, however, mentions the use of random number generators as part of the process.

Applicants filed this Information Disclosure Statement ("IDS") before the mailing date of a first Office action on the merits. As a result, no fee should be required to file this IDS. However, if the Patent Office determines that a fee is required for Applicants to file this IDS, please charge any such fees, or credit overpayment, to Deposit Account No. 02-4550. A **duplicate** copy of this Information Disclosure Statement is enclosed.

The filing of this IDS shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

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Docketing

Attorney Docket Number	1011-67627-01
Application Number	10/781,031
Filing Date	February 17, 2004
First Named Inventor	Rajski
Art Unit	2124
Examiner Name	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

U.S. PATENT DOCUMENTS

NOTE: If this application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55).

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
		4,536,881	8.20.1985	Kasuya
		5,202,889	4.13.1993	Aharon et al.
		5,701,308	12.23.1997	Attaway et al.
		5,870,476	2.9.1999	Fischer
		5,872,793	2.16.1999	Attaway et al.
		5,883,906	3.16.1999	Turnquist et al.
		5,983,380	11.9.1999	Motika et al.
		6,122,761	9.19.2000	Park
		6,829,740	12.7.2004	Rajski et al.

U.S. PATENT APPLICATION DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Number	Filing Date	Name of Applicant
		09/620,021	7.21.2000	Rajski et al.

FOREIGN PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee
		Europe	EP 0372226	6.13.1990	Bardell
		Europe	EP 0438322	7.24.1991	Murase
		Europe	EP 0481097	4.22.1992	Diebold et al.

EXAMINER SIGNATURE:	DATE CONSIDERED:

* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.

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FOREIGN PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee
		Japan	JP 4-236378	8.25.1992	Diebold et al.
		Japan	JP 9-130378	5.16.1997	Fischer
		Europe	EP 0887930	12.30.1998	Tarrab et al.
		Japan	JP 11-153655	6.8.1999	Park

Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
		Bassett et al., "Low-Cost Testing of High-Density Logic Components," *IEEE Design & Test of Computers*, pp. 15-28 (April 1990).
		Fagot et al., "On Calculating Efficient LFSR Seeds for Built-In Self Test," *IEEE*, pp. 7-14 (1999).
		Hellebrand et al., "Generation of Vector Patterns Through Reseeding of Multiple-Polynomial Linear Feedback Shift Registers," *IEEE International Test Conference*, pp. 120-129 (1992).
		Langdon, Jr., "An Introduction to Arithmetic Coding," IBM J. Res. Develop., Vol. 28, No. 2, pp. 135-149 (March 1984).
		Wang, "BIST Using Pseudorandom Test Vectors and Signature Analysis," *IEEE Custom Integrated Circuits Conference*, pp. 1611-1618 (1998).

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